



# John T. Anderson Engineering Note

**Date:** 9/22/98  
**Rev Date:** ~~10/16/98~~ 1/6/99<sup>1</sup>  
**Project:** CFT Front End Axial  
**Doc. No:** a980922a  
**Subject:** Software map of board

## ***Introduction***

The CFT Axial board is connected to the rest of the D0 experiment by a MIL-STD 1553 interface. In this protocol, each CFT board looks like one **Remote Terminal (RT)**, with up to 30 registers. Each of the 30 registers should be viewed as a FIFO up to 32 words deep. Whenever a particular register is accessed, it is read from one to 32 times by the host software. Each register is sixteen bits wide.

Jamieson Olsen has written a couple of notes describing the implementation of the 1553 interface; this document attempts to look at the non-1553 side of his logic to show how the various sections of the CFT Axial board map out.

## ***Board Architecture – Hardware Perspective***

The CFT Axial board has a small microcontroller – a PIC14000 – whose basic function is to provide a simplified interface to the various DAC and ADC channels on the board. A secondary function of this microcontroller is to allow each Right-Hand CFT board to act as a cassette closed-loop temperature control system in the event that remote temperature control is not sufficient. A tertiary function is to provide a control mechanism for sequencing power application to the SIFT and SVX chips on the CFT board.

This microcontroller is attached to the main board data bus via a dual-port memory. The dual-port memory allows the 1553 interface to access the microcontroller data in 16-bit chunks, but allows the microcontroller to use the more convenient byte-wide architecture on its side. Further, the dual-port decouples the timing of the two systems. Figure 1 shows a quick sketch of the microcontroller and its interface.

## ***Board Architecture – Software Perspective***

The CFT Axial board contains numerous functional blocks, but many of these are only indirectly connected to the software. Thus, the software perspective of the board is very different from the schematic's block-level view. As seen by the software, the CFT Axial card looks like a base address register and a single memory location.

Register Address	Register Name	Functional Description	Depth on reads	Depth on writes
0	BASE_ADDR	Register which contains base address of window into board memory space, accessed through register 1	One word	One word
1	DATA_PORT	I/O port through which 1553 accesses up to 32 locations of board dual-port RAM	Up to 32	Up to 32

**Table 1**

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<sup>1</sup> Added items related to control of Clock Generator CPLD.

The 1553 software loads the BASE\_ADDR register with the address within the dual-ported RAM that is to be modified, and then writes up to 32 words to the DATA\_PORT register. The 1553 interface keeps a local count of how many words are written or read and drives the internal address bus appropriately.

## Internal Memory Map

The CFT Axial Board actually contains 64K X 16 bits of dual-port RAM. Table 2 shows what the various locations do. Descriptions of individual fields and bitmaps follow.

Addresses	Function
0x0000 – 0x003F	64 X 16 storage space for values to store in DACs 0 – 63.
0x0040 – 0x007F	64 X 16 storage space for ADC readbacks of DACs 0 –63.
0x0080 – 0x0087	Analog readback of eight Cryo Sense Resistors, one per Flex Cable.
0x0088	Demand temperature for Cryostat.
0x0089	Board temperature readback
0x008A	Local Vcc readback for system monitoring purposes.
0x008B	Local 3.3V readback for system monitoring purposes.
0x008C	Local +12V readback for system monitoring purposes.
0x008D	Local –12V readback for system monitoring purposes.
0x008E – 0x008F	Flash Ram Sector Checksum.
0x0090	Flash Ram Sector Number – which sector is to be programmed or read out.
0x0091	Address of beginning of Sector Shadow area within this RAM
0x0092	Length of Sector Shadow area within this RAM to be transferred to/from Flash RAM.
0x0093 – 0x0097	Control values for Clock Generator subsection of board.
0x0098 - 0x009F	Digital control values for MCMs (gain switches)
0x00A0- 0x00AF	Microcontroller Command Block (where to store microcontroller commands)
0x00B0 – 0x00BF	Microcontroller Status Block (results of commands)
0x00C0 – 0x00CF	Control values for Virtual SVX subsection of board.
0x00D0 – 0x00FF	List of addresses where FPGA data block start, sufficient for 64 devices on board.
0x0100 – 0x013F	List of addresses where FPGA data blocks stop, sufficient for 64 devices on board.
0x0140 – 0x015F	Bitmap to store Fake Event Data for serial download into Latch CPLDs
0x0160 – 0x017F	Bitmap to store Captured Event Data from serial upload of Latch CPLDs
0x0180 – 0x01FF	Reserved.
0x0200 – 0x02FF	Calibration constant area.
0x0300 – 0xFFFF	Sector Shadow RAM area.

**Table 2**

## Microcontroller Command Processing

Upon power up the microcontroller resets and then enters an idle loop. As part of the reset, locations 0x00A0 through 0x00AF (Microcontroller command block) and locations 0x00B0-0x00BF (Microcontroller Status Block) are cleared to zeroes. In the idle loop, the microcontroller polls location 0x00AF, and if it is non-zero, interprets the values found in 0x00A0 through 0x00AE as a command sequence. The commands stored in these locations are processed in order. After the queue is empty the microcontroller re-enters the idle state.

## Microcontroller Command Format

Each 16-bit value is interpreted as a command value for the microcontroller. The lower 5 bits are the actual command, and at present the upper bits are ignored. The commands implemented are as shown in Table 3:

Value	Command Function	Status change
0	No-op	N/A
1	Begin download FPGAs from data stored in Flash Ram.	Reports 'Busy' until complete.
2	Erase single sector of Flash Ram; which sector to erase must have been previously stored in location 0x0090.	Reports 'Busy' until complete.
3	Copy single sector of Flash Ram to Sector Shadow area; which sector to copy must have been previously stored in location 0x0090.	Reports 'Busy' until complete.
4	Copy Sector Shadow area to Flash Ram. Which sector to reprogram must have been previously stored in location 0x0090.	Reports 'Busy' until complete.
5	Bulk erase entire Flash Ram.	Reports 'Busy' until complete.
6	Calculate checksum of a single sector of Flash Ram and store in checksum area (addresses 0x008E and 0x008F). Sector to checksum must have been previously stored in location 0x0090.	Reports 'Busy' until complete.
7	Calculate checksum of Sector Shadow area and store in checksum area.	Reports 'Busy' until complete.
8	Update all DACs on board with new data from locations 0x0000 through 0x003F.	Reports 'Busy' until complete.
9	Perform analog conversion of all DAC channels.	Reports 'Busy' until complete.
10	Perform analog conversion of board status channels (Update locations 0x0089 – 0x008D)	Reports 'Busy' until complete.
11	Perform analog conversion of cassette temperatures (Update locations 0x0080 – 0x0087)	Reports 'Busy' until complete.
12	Copy virtual SVX operating parameters from dual-port RAM to device.	Reports 'Busy' until complete.
13	Copy clock controller operating parameters from dual-port RAM to device.	Reports 'Busy' until complete.
14	Download Fake Event Data to Latch CPLDs	Reports 'Busy' until complete.
15	Upload Latch CPLDs into dual-port RAM	Reports 'Busy' until complete.
16	Zero out ADC readback values (0x0040-0x007F)	Reports 'Busy' until complete.
17	Zero out board status channels (0x0089-0x008D)	Reports 'Busy' until complete.
18	Zero out cassette temperature measurements (0x0080-0087)	Reports 'Busy' until complete.
19	Zero out Sector Shadow area of dual-port RAM	Reports 'Busy' until complete.
20	Reset all DAC's to zero (bulk reset) and zero out DAC demand section of dual-port RAM	Reports 'Busy' until complete.
21	Turn on power to MCMs	Reports 'Busy' until complete.
22	Turn off power to MCMs	Reports 'Busy' until complete.
23	Load new gain control values to MCMs from dual-port RAM	Reports 'Busy' until complete.
24	Update Clock Controller Status from CPLD to dual-port RAM	Reports 'Busy' until complete.
254-31	Reserved for future use.	'Illegal Command' bit set in status.

**Table 3**

The microcontroller reads and processes the command stored in location 0x00A0 first and continues to process forward until it finds a no-op. As each command is processed the RAM location is re-set to no-op. After processing the entire set it then returns to polling location 0x00AF. This allows the 1553 control system to load up a set of commands, set the board in motion, and then simply poll to see if the sequence is complete. Location 0x00AF (COMMAND\_CONTROL) has a simple format as shown in Table 4. The microcontroller polls this location, and if it is non-zero, first zeroes the register and then performs the function requested. Only one bit in the COMMAND\_CONTROL register may be set at a time. If multiple bits are set, the microcontroller will ignore the request. During the operation of a sequence of commands, location 0x00AF is sampled prior to the execution of each command in sequence to see if the ABORT bit is set. If so, the rest of the list is ignored.

Bit	Function on Write
15..8	Reserved for future use.
7	If set, tells microcontroller to exit Cryo Loop subroutine and return to idle loop.
6	Execute commands as previously stored in command list.
5	Perform power-up reset sequence (reboot).
4	Enter Cryo Loop subroutine; ignore standard command processing until told to exit.
3	Clear Command and Status areas to all zeroes
2	ABORT; if set, aborts execution of sequence in progress
1	Copy all internal microcontroller calibration constants to dual-port RAM
0	Copy new internal microcontroller calibration constants from dual-port RAM

**Table 4**

### ***Microcontroller Status Information***

Memory locations 0x00B0 through 0x00BF are reserved for microcontroller status. Location 0x00B0 is a bitmap of general status and 0x00B1 through 0x00BF are used for additional, command-specific information. Table 5 gives the bitmap of location 0x00B0:

Bit	Meaning if set
15..8	Reserved.
7	DAC update in progress.
6	ADC conversion(s) in progress.
5	Status valid. Cleared when a command begins to process, set when a command is finished.
4	Last command was RESET.
3	In Cryo Loop mode.
2	Sequence was aborted.
1	Illegal command number.
0	Busy processing a command.

**Table 5**

### ***DAC and ADC storage spaces***

Addresses 0x0000 through 0x003F hold 64 eight-bit values which correspond to each of the 64 DACs on the CFT board. The lower eight bits are valid and the upper eight bits are ignored. Addresses 0x0040 through 0x007F hold the ADC readback values of the 64 DACs and/or VLPC current sensors. In each of the eight blocks of ADC data, the last channel of the ADC corresponds not to the Test Charge voltage, but rather reads back the current in the VLPC supply.

### ***Analog readback of eight Cryo Sense Resistors, one per Flex Cable***

Each location simply contains the 16 bit readback of the voltage sensed.

### ***Demand temperature for Cryostat***

A sixteen bit value, units still TBD.

### ***Board temperature readback***

A sixteen bit value taken from the local temperature sensor within the microcontroller. Units TBD.

### ***Local Vcc readback for system monitoring purposes.***

A sixteen bit analog conversion of the Vcc voltage, units TBD.

### ***Local 3.3V readback for system monitoring purposes.***

A sixteen bit analog conversion of the 3.3V supply voltage, units TBD.

### ***Local +12V readback for system monitoring purposes.***

A sixteen bit analog conversion of the +12V supply voltage, units TBD.

### ***Local –12V readback for system monitoring purposes.***

A sixteen bit analog conversion of the –12V supply voltage, units TBD.

### ***Flash Ram Sector Checksum.***

A 32 bit checksum of one sector of the Flash Ram, per Jamieson's note #xxxxxx.

### ***Flash Ram Sector Number – which sector is to be programmed or read out.***

A simple index value from 0 to 127, indicating which 32K sector of the 4 megabytes of data in the Flash Ram is to be modified or accessed.

### ***Address of beginning of Sector Shadow area within this RAM***

A base address allowing 1553 to store excess data where it wants to within the dual-port RAM.

### ***Length of Sector Shadow area within this RAM to be transferred to/from Flash RAM.***

The 'transfer length' for any Flash access. This many bytes from the base address (see immediately above) will be transferred.

### ***Control values for Clock Generator subsection of board.***

———Reserved for offset values to allow board-by-board fine tuning.——— Location 0x0093 is copied from the DPRAM to the Clock Generator's Event Delay Register. Location 0x0094 maps to the Clock Control Register. Location 0x0095 maps to the Clock Generator Status Register.

### ***Digital control values for MCMs (gain switches)***

Set of eight five-bit values for discriminator gain, SVX gain, etc, one per MCM.

***Control values for Virtual SVX subsection of board.***

TBD.

***List of addresses where FPGA data blocks start, sufficient for 64 devices on board.***

Allows for tight packing of Flash RAM data.

***List of addresses where FPGA data blocks stop, sufficient for 64 devices on board.***

Allows for tight packing of Flash RAM data.

***Bitmap to store Fake Event Data for serial download into Latch CPLDs***

An 'event' is 480 (512) bits, which are time-multiplexed into the Latch CPLDs. This area allows 1553 to store an event pattern for serial download into the Latch CPLDs by the microcontroller. This allows for some testing of the Trigger Logic.

***Bitmap to store Captured Event Data from serial upload of Latch CPLDs***

A reverse serial capture, to allow the CFT board to store the raw data generated by Bruce's test board.

***Reserved.***

***Calibration constant area.***

Shadow area for microcontroller analog calibration constants.

***Sector Shadow RAM area.***

Area in dual-port RAM which stores copy of sector to be transferred to/from the Flash RAM.